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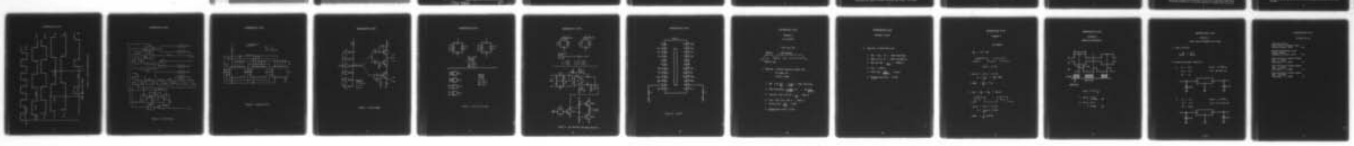

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Technical Report: NAVTRAEQUIPCEN IH-267

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ELECTRONIC CONTROL FOR 360 DEGREE NONPROGRAMMED VISUAL DISPLAY

Electronics and Acoustics Laboratory
Naval Training Equipment Center
Orlando, Florida 32813

November 1976

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ELECTRONIC CONTROL FOR 360 DEGREE NONPROGRAMMED VISUAL DISPLAY

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November 1976

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An electronic control system is designed for a 360 degree nonprogrammed visual display. Synchronizing signals for various system components are developed based on an analysis of the system requirements. Discussion of state-of-the-art logic required is given and detailed circuitry is shown for system implementation.

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SECTION I

INTRODUCTION

Research and Technology Task No. 7719, 360 Degree Nonprogrammed Visual Display, calls for the fabrication of a feasibility model of a 360 degree non-programmed visual display. The display relies on a group of 12 charge coupled device (CCD) linear arrays as pickup devices and 12 lasers as output devices. Various rotating components are also incorporated in the system. In order that the CCD arrays, lasers, and rotational system components work together properly, they must be synchronized. The design of an electronic control system providing synchronizing signals to the display system components is presented in this report. A display system analysis yields the required frequency of the master clock and countdown circuits are determined for the various components which require synchronization. Conclusions are reached regarding the confidence level of the electronic control system, since the frequencies required demand the use of state-of-the-art logic. Recommendations are made on an alternative lower frequency and the effect of lower frequency clocks on the original system is given.

SECTION II

STATEMENT OF THE PROBLEM

Design electronic control circuits to provide common synchronizing pulses to the pickup elements (CCDs), the display elements (lasers), and the rotational elements which provide the vertical and horizontal sweeps to the scanning and writing beams.

SECTION III

SYSTEM ANALYSIS

The block diagram in figure 1 shows the pickup-display system. The electronic control system must provide synchronous clocking pulses to control (1) CCD outputs, (2) the laser scanner, (3) rotation prism, and (4) derotation prism noted in figure 1. A video amplifier to provide modulation signals to the laser modulator is also required. The fundamental requirements fixing the clock frequencies for the electronic control system are:

a. Three minutes of arc between raster lines

b. Thirty Hertz frame rate

c. Two to one interlace

d. Twelve CCD line sensors and 12 laser line outputs

Since there are 360 degrees in the display,

then

$$(360 \times 60)/3 = 7200 \text{ lines are required per frame}$$

Since there are 12 CCDs (and lasers)

$$7200/12 = 600 \text{ lines}$$

per CCD are required per frame. Since the frame rate is 30 Hertz, and the number of pixels per CCD is 1728

$$600 \times 30 \times 1728 = 31.104 \text{ MHz}$$

is required clock frequency to pulse out the video from the CCDs. Since some transfer time (about 2,000 nanoseconds) is needed to transfer the charge into the shift register, the required clock frequency is about 32 MHz. Since 32 MHz is the highest required frequency, the minimum input master clock is 64 MHz.

The laser scanner is a twelve faceted mirror each of which puts out 12 lines per revolution - 144 lines in all.

Since

$$7200 \times 30 = 216,000$$

lines are required, the laser scanner must rotate at

$$21600/144 = 1500$$

revolutions per second or 90,000 revolutions per minute. The nearest

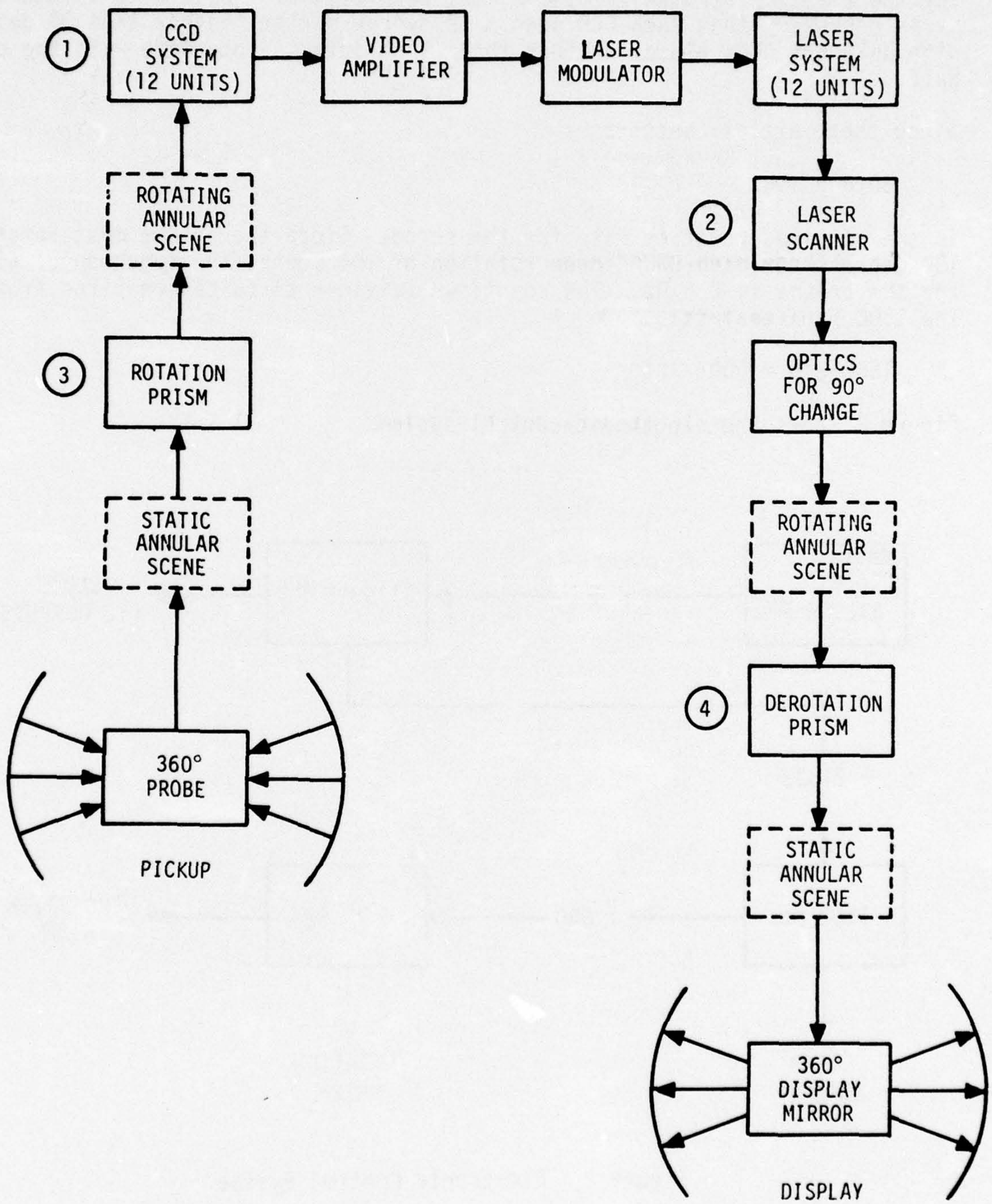


Figure 1. Pick-up Display System Using CCD Sensors and Laser Display System For 360° Cylindrical Display

integral dividend to 32 MHz, which will yield 1500 rps, is 31.9995 MHz. That is, if we divide 31.9995 MHz by 21333, the result is 1500 Hz which will be the synchronizing signal for the rotating laser scanner. Synchronizing signals for the rotation/derotation prisms must be provided. For a 2 to 1 interlace, it is necessary that each CCD scan a 60 degree sector (rather than 30 degree) with half the CCDs placed so that their line outputs interlace with the other half.

Since there are six sectors

30/6 = 5 Hz

is the required rotation rate for the scene. Since the prisms must rotate 180 degrees for each 360 degree rotation of the scene, the synchronous signal for the prisms is 2.5 Hz. The countdown (divider circuits) required from the 1500 Hz signal is

1500/2.5 = 600

Figure 2 shows the electronic control system.

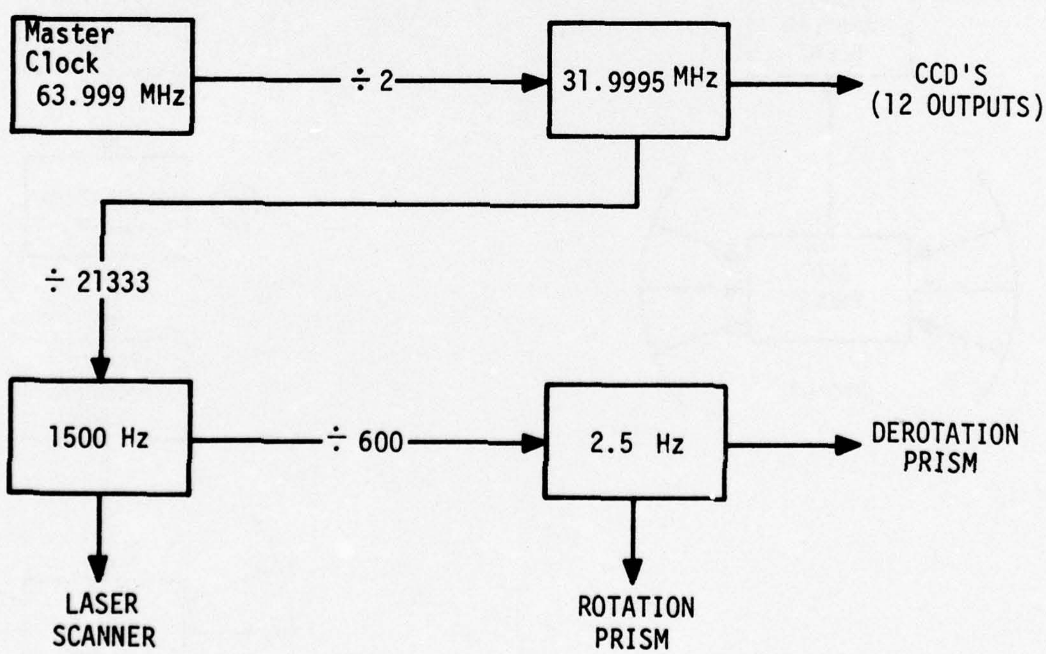


Figure 2. Electronic Control System

Detailed circuitry will be shown using a 60 MHz master clock. Sixty MHz is used as an example because of the inability to forecast the exact rotation rate of the laser scanner (90,000 rpms in exercise above) to be delivered from the manufacturer.

The high-clocking requirements of this design produce pulses with time lengths in the area of the propagation delays of state-of-the-art logic. The only possible choices of logic which can be used are:

a. Emitter Coupled Logic (ECL) - smallest propagation delay, 2-3 ns

b. Schottky - propagation delay 5 - 10 ns.

ECL voltage level is not compatible with that of other circuitry that must be used so Schottky logic must be used.

Once the choice was made to use Schottky logic, a study of each chip was made for propagation delays versus the final clocking requirements. This is shown in figures 3 and 4. Figure 3 is a timing diagram of the clocking required for the charge coupled device, CCD 121. Figure 4 shows the typical delay error due to propagation times.

Figure 5 is a block diagram of the drive circuit and shows the gates that can be introduced to correct the delay error shown in figure 4.

a. Counters A, B, and C are included in this design to have the option of a synchronous or asynchronous system. With the switch on EXT. START, a command-pulse from an external source controls the read cycle. With the switch on FREE-RUN, a new cycle is initiated at the end of the 1728 element readout from the counters.

b. The five drive clocks are Ø1, Ø2, ØR, ØXA, ØXB. The correct sequence of the clocks is shown in figure 3.

c. A decision was made to use one clock source for all the drive circuitry to keep any error down to a minimum. A 15 MHz clock is available for the mirror and prism drive systems. This clock can be divided down to the frequencies that are required by the manufacturers of these systems. This still has to be looked into to determine what type of motor drive circuitry is required.

Figures 6 through 9 describe the detailed circuitry required for the CCD clocking and output amplifier.

Figure 10 shows the CCD chip and external connections.

Appendix A is an analysis of the minimum input clock that is required for a resolution of three minutes and four minutes between scan lines. The operation of the CCD 121 is going to be borderline at these clocking rates and may present a problem of integration time, i.e., the time allowed for the photosites to collect charge. If the time is too short, the output signal may be very low and difficult to pull out of the dark-signal noise. The output amplifier is a low noise type with a variable gain and can be

trimmed for higher output signals.

Appendix B details the CCD 121 loading requirements at the required clocking rate. Peak currents of 700 ma must be considered for the power supply requirements.

Appendix C details the bandwidth requirement for the amplifier system and laser modulator. A minimum bandwidth of 40 MHz would be a safe figure to use for the specifications when purchasing the modulator and modulation drive amplifier.

Appendix D details the power supply requirements and the voltage regulators to be used. The current drain is for one complete CCD 121 system. If there will be 12 CCDs, it is recommended that three power supplies per system be purchased.

The clocking system, CCD 121 Chip, and the output amplifiers, should be contained on a printed circuit board that is designed for high frequency operation. The board should have a ground plane, a Vcc plane, and use decoupling capacitors; 0.047 µf mounted next to each logic chip and 10 µf for each voltage source. Due to the high frequency requirements, the design of this board should be carefully planned by someone with expertise in board layouts.

SECTION IV

CONCLUSIONS

An electronic control circuit is required for the synchronous operation of the CCDs, the laser scanner, and the rotation-derotation prisms of the 360 degree visual display system. The master clock frequency of approximately 60 MHz demands the use of state-of-the-art Schottky logic. The high frequency required may degrade the performance of the CCD arrays to the point where a relaxation of the display system requirements will be necessary. Appendix A gives the frequencies for a three minute arc separation and those for a four minute arc separation. Since both these separations are better than currently available on wide angle visual systems, further relaxation for a feasibility model does not seriously affect a decision to proceed with the project.

SECTION V

RECOMMENDATIONS

It is recommended that consideration be given to using a less stringent requirement than three minutes of arc separation of the TV raster lines due to the critical propagation delays of the clocking circuitry. It is recommended that personnel of the Electronics and Acoustics Laboratory be kept informed of the progress in purchasing the various system components so that testing and system design can be continually updated as necessary as purchases are made.

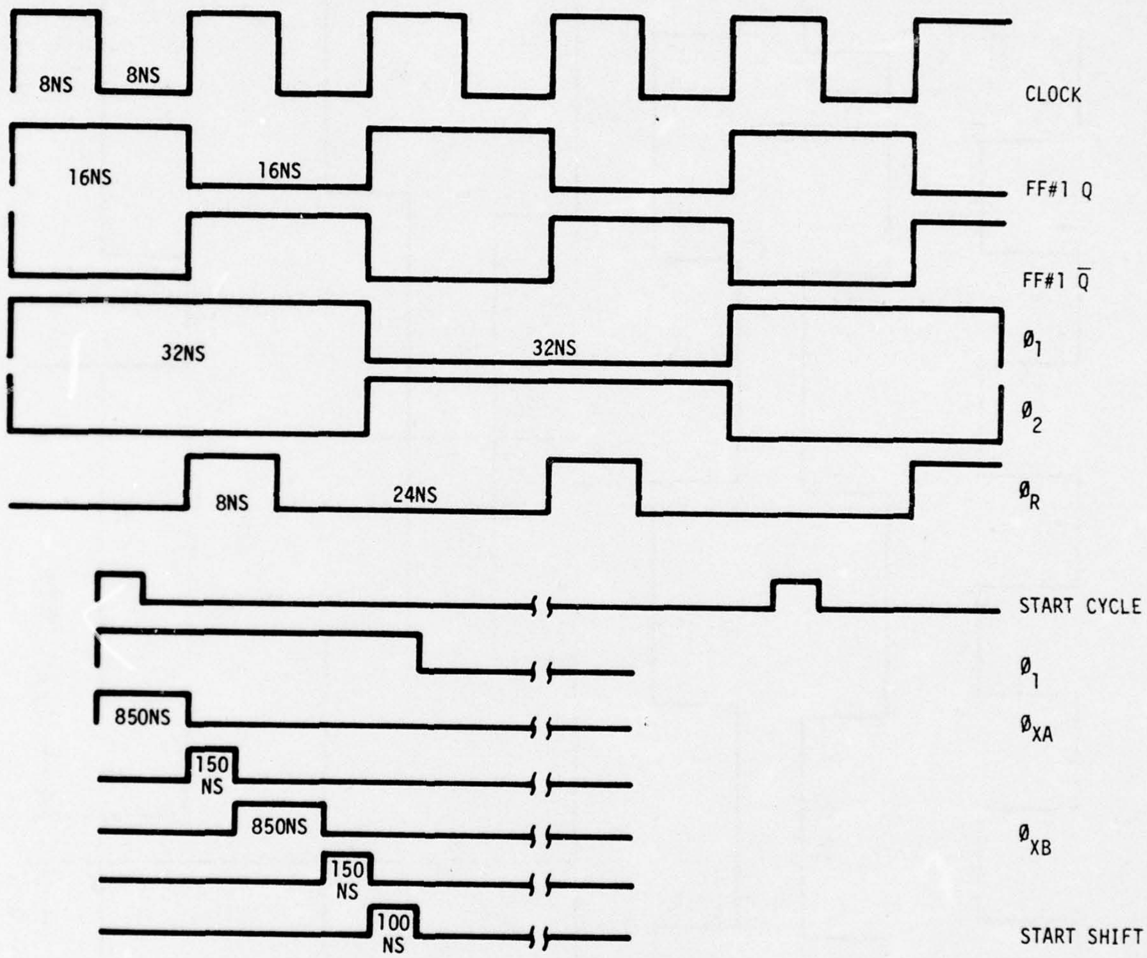


Figure 3. Timing Diagram

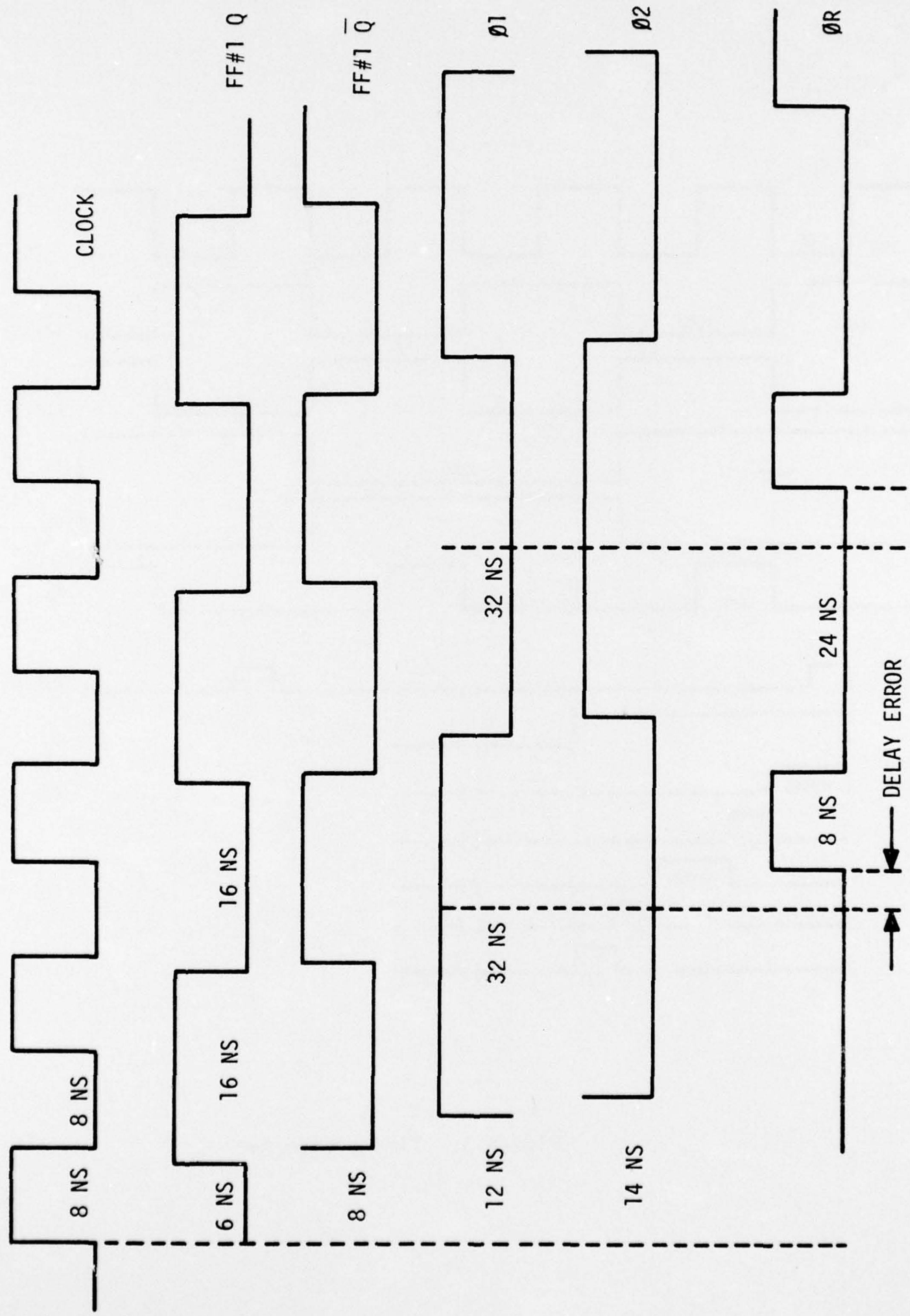


Figure 4. Typical Propagation Delays

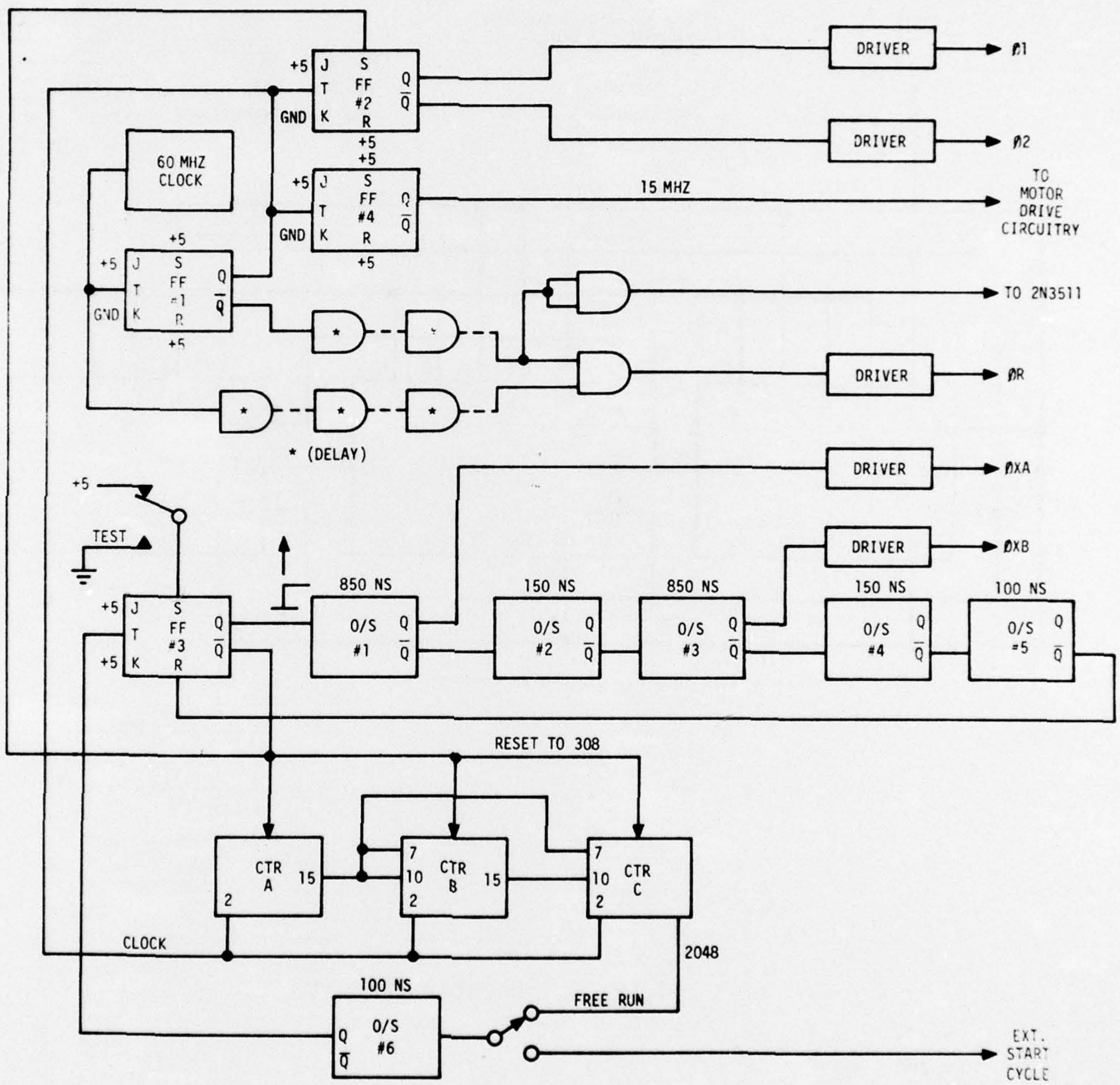


Figure 5. Drive Circuit

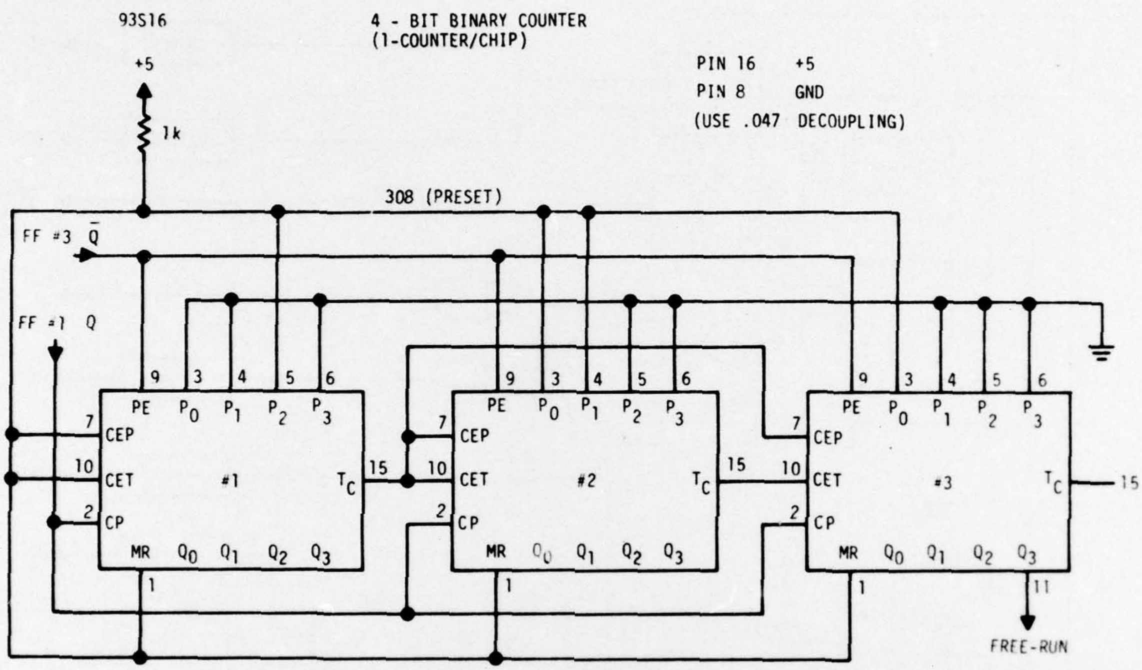


Figure 6. Counter Circuit

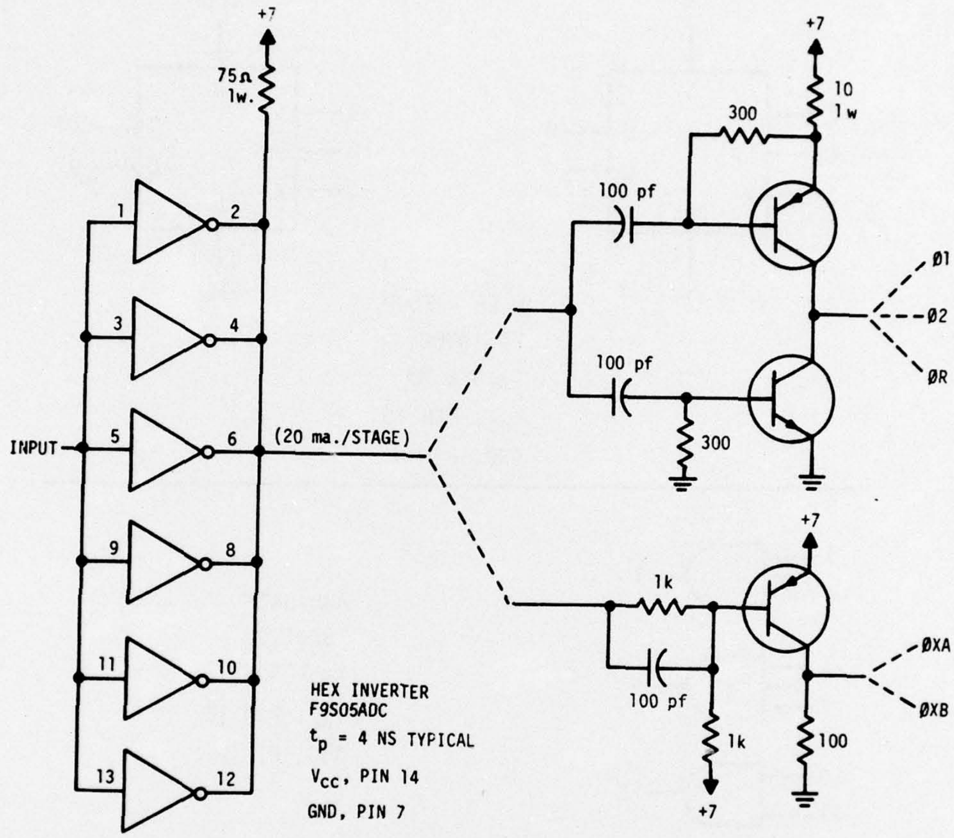


Figure 7. Driver Stages

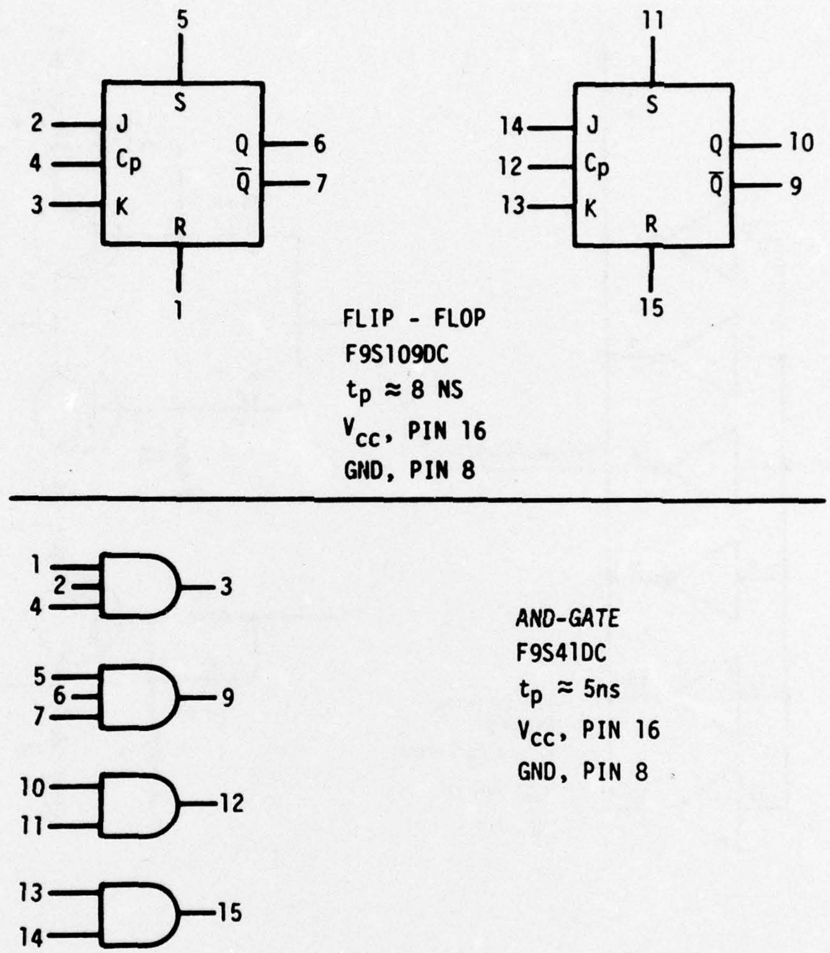
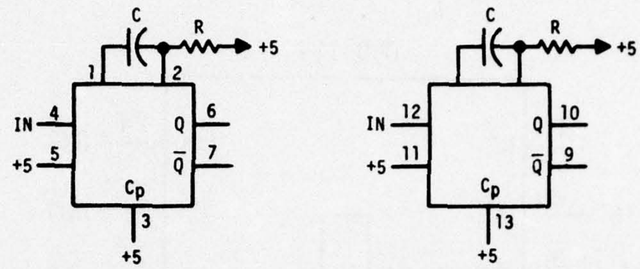


Figure 8. Flip Flip and Gates



DUAL ONE-SHOT
9602 DC
Vcc, PIN 16 (*USE 0.01 μf CAP. BETWEEN Vcc & GND)
GND, PIN 8

1. T = 850 ns R = 27k, C = 100 pf
2. T = 150 ns R = 7.5 k, C = 22 pf
3. T = 100 ns R = 5 k, C = 22 pf

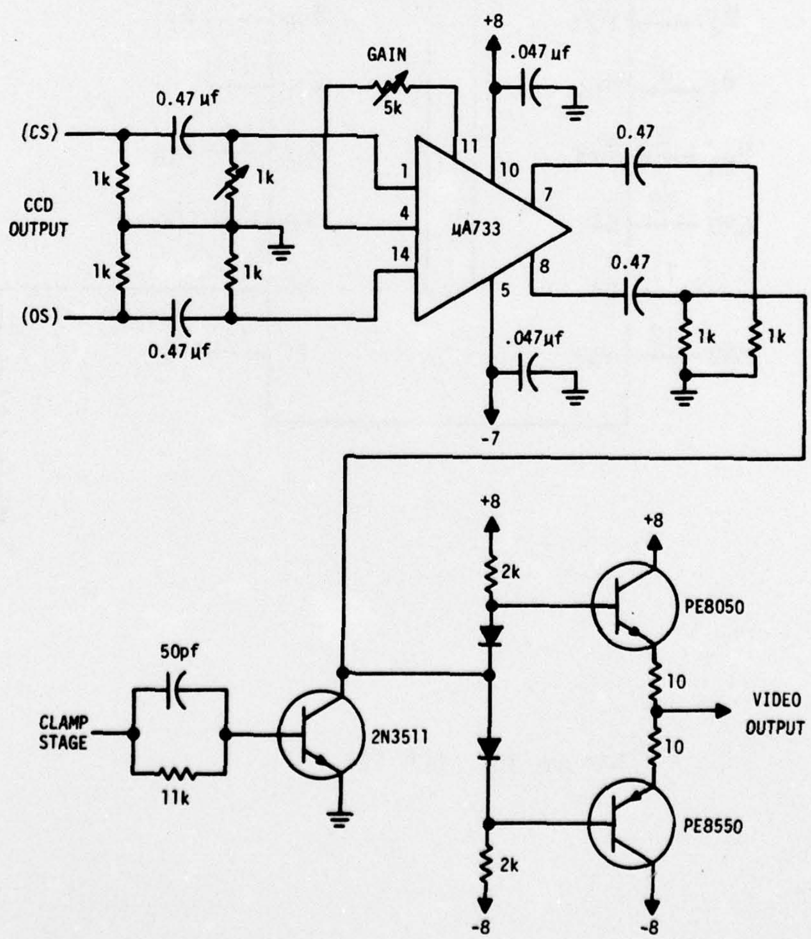


Figure 9. Dual One-Shot and Output Amplifier

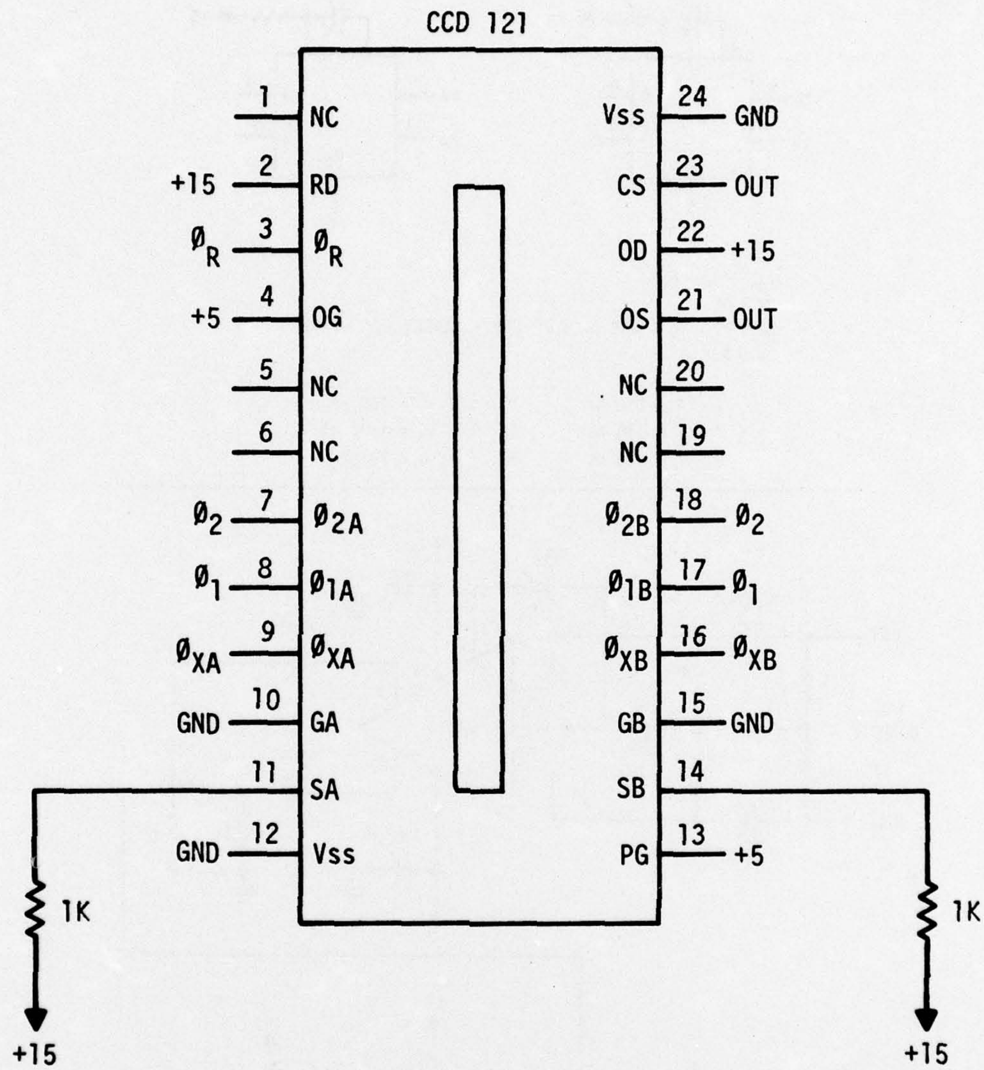
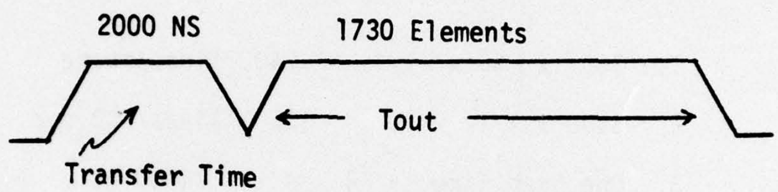


Figure 10. CCD 121

APPENDIX A

CCD CLOCKING

Total Scan Time



I. Required: 3 minute resolution between lines

30 frames /sec

12 CCD's /frame

1. $360° \times 60 \ \frac{\text{min}}{\text{Deg}} \times \frac{1 \text{ line}}{3 \text{ min}} = 7200$ lines/frame
2. 7200 lines/frame $\times \frac{1 \text{ frame}}{12 \text{ CCD's}} \times 30 = 18\text{K} \ \frac{\text{lines}}{\text{CCD Sec}}$
3. Time for 1 total CCD scan $= \frac{1}{18\text{K}} = 5556$ NS
4. Tout = Total scan - 200 ns = 53556 ns
5. Clocking rate: $\frac{1730}{\text{Tout}} = 32$ MHz
6. <u>Minimum</u> Input clock is 64 MHz

APPENDIX A (Cont)

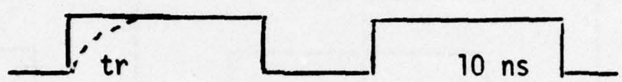
II. Required: 4 Minute Resolution

1. $360 \times 60 \times 1/4 = 5400$ lines/frame
2. $5400 \times 1/12 \times 30 = 13500$ lines/CCD sec
3. One Scan Time $= \frac{1}{13500} = 74000$ ns
4. Tout = 72000 ns
5. Clock rate: $\frac{1730}{72000\ \text{NS}} = 24$ MHz
6. Minimum Input Clock = 48 MHz

APPENDIX B

CCD LOADING

$C\varnothing_r = 1$ pf load



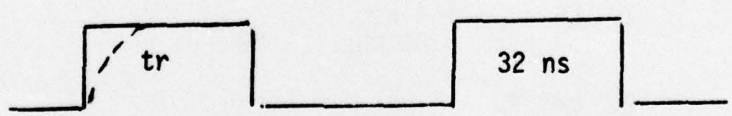
$$T_{rise} = 2.2\ RC$$

1. Let $tr = 2.2\ \text{ns} = 2.2\ RC$

$$R = \frac{1\ \text{ns}}{C} = 1000\ \text{ohms}$$

$$I\ \text{peak} = \frac{7V}{1K} = 7\ \text{ma}$$

2. $C\varnothing_1 = C\varnothing_2 = C\varnothing_x = 400$ pf



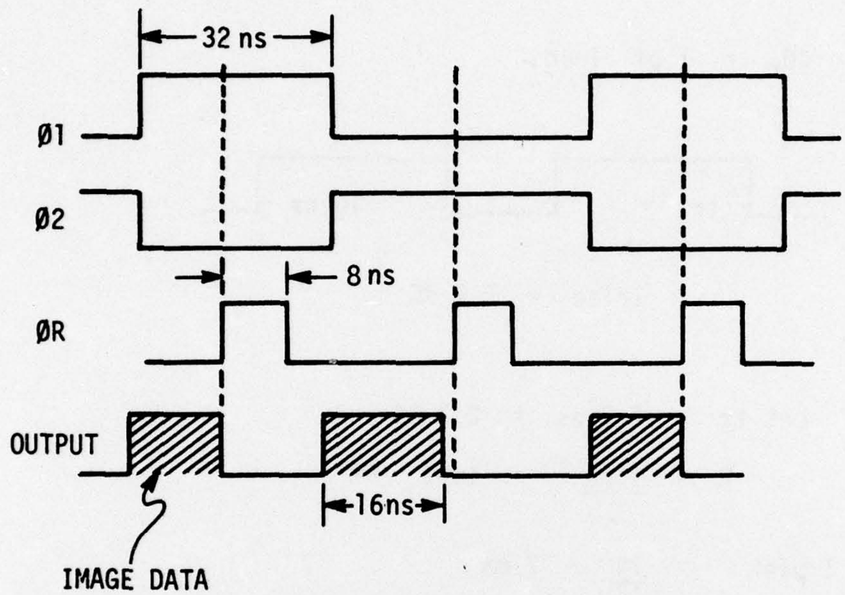
Let $tr = 10\ \text{ns} = 2.2\ RC$

$$R = \frac{5\ \text{ns}}{C} \approx 12\ \text{ohms}$$

$$I\ \text{peak} = \frac{7}{12} \approx 700\ \text{ma}$$

APPENDIX C

BANDWIDTH REQUIREMENTS



$$T_{rise} = 2.2\ RC = \frac{1}{3f}$$

1. Let T_r = 4 ns
   f = 80 MHz BW

2. Let T_r = 8 ns

   F = 40 MHz BW

APPENDIX D

POWER SUPPLY REQUIREMENT PER SYSTEM

I. *Logic Circuitry:*

Vcc	=	+5 V
I Drain	=	700 ma

II. Drivers and Output Amplifier

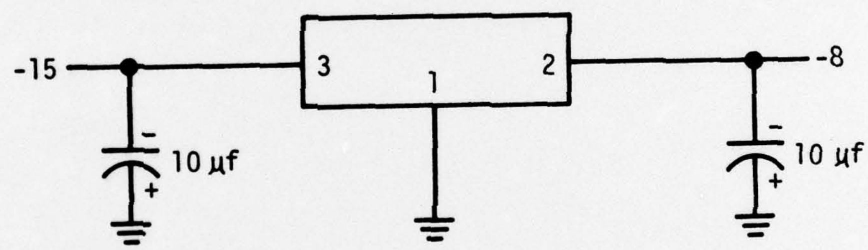
a. Ei = +15 V

Vcc = +8 V

ID = 1A.

Device: μ A 7808 UC

* Use 10W Heat Sink



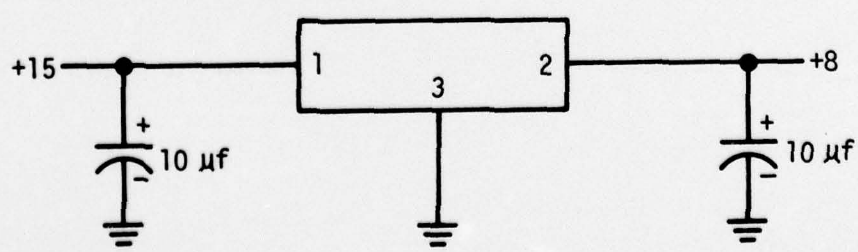
b. Ei = -15 V

Vcc = -8 V

ID = 300 ma

Device: μ A 7908 UC

* Use 10 W. Heat Sink



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